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DATA SHEET

UDA1331H
Universal Serial Bus (USB) Audio Playback Peripheral (APP)

Preliminary specification
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1998 Oct 06

Philips Semiconductors

PHILIPS

Universal Serial Bus (USB) Audio Playback Peripheral (APP)

UDA1331H

FEATURES

General

- Universal Serial Bus (USB) stereo Audio Playback Peripheral (APP) system with adaptive (5 to 55 kHz) 20-bits digital-to-analog conversion and filtering
- USB-compliant audio and Human Interface Device (HID)
- Supports 12 Mbits/s full-speed serial data transmission
- Supports multiple audio data formats (8, 16 and 24 bits)
- Supports headphone and line output
- Fully automatic ‘Plug-and-Play’ operation
- High linearity
- Wide dynamic range
- Superior signal-to-noise ratio (typical 95 dB)
- Low total harmonic distortion (typical 90 dB)
- 3.3 V power supply
- Efficient power management
- Low power consumption
- On-chip master clock oscillator, only an external crystal is required
- Partly programmable USB descriptors and configuration via I^{2}C-bus.

Sound processing

- Separate digital volume control for left and right channel
- Soft mute
- Digital bass and treble tone control
- External Digital Sound Processor (DSP) option possible via standard I^{2}S-bus or Japanese digital I/O format
- Selectable clipping prevention
- Selectable Dynamic Bass Boost (DBB)
- On-chip digital de-emphasis.

Document references

- *“USB Specification”*
- *“USB Common Class Specification”*
- *“USB Device Class Definition for Audio Devices”*
- *“Device Class Definition for Human Interface Devices (HID)”*
- *“USB HID Usage Table”*.

APPLICATIONS

- USB monitors
- USB speakers
- USB headsets
- USB telephone/answering machines
- USB links in consumer audio devices.

GENERAL DESCRIPTION

The UDA1331H is a stereo CMOS digital-to-analog bitstream converter designed for USB-compliant audio playback devices and multimedia audio applications. The UDA1331H is an adaptive asynchronous sink USB audio device with a continuous sampling frequency (f_s) range from 5 to 55 kHz. It contains a USB interface, an embedded microcontroller and an Asynchronous Digital-to-Analog Converter (ADAC).

The USB interface is the interface between the USB, the ADAC and the microcontroller. The USB interface consists of an analog front-end and a USB processor. The analog front-end transforms the differential USB data to a digital data stream. The USB processor buffers the input and output data from the analog front-end and handles all low-level USB protocols. The USB processor selects the relevant data from the universal serial bus, performs an extensive error detection and separates control information (input and output) and audio information (input only).

The control information becomes accessible at the microcontroller. The audio information becomes available at the digital I/O output or is fed directly to the ADAC.

The microcontroller handles the high-level USB protocols, translates the incoming control requests and manages the user interface via General Purpose (GP) pins and an I²C-bus. The firmware for the microcontroller must be located in an external (E)PROM.

The ADAC enables the wide and continuous range of input sampling frequencies. By means of a Sample Frequency Generator (SFG), the ADAC is able to reconstruct the average sample frequency from the incoming audio samples. The ADAC also performs the sound processing. The ADAC consists of FIFO registers, a unique audio feature processing DSP, the SFG, digital up-sampling filters, a variable hold register, a Noise Shaper (NS) and a Filter Stream DAC (FSDAC) with integrated filter and line output drivers. The audio information is applied to the ADAC via the USB processor or via the digital I/O input.

An external DSP can be used for adding extra sound processing features via the digital I/O-bus.

The UDA1331H supports the standard I²S-bus data input format and the LSB-justified serial data input format with word lengths of 16, 18 and 20 bits.

The wide dynamic range of the bitstream conversion technique used in the UDA1331H guarantees a high audio sound quality.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DD}	supply voltage	note 1	3.0	3.3	3.6	V
$I_{DD(tot)}$	total supply current		–	50	–	mA
$I_{DD(ps)}$	supply current in power-save mode		–	18	–	mA
Dynamic performance DAC						
$\frac{THD + N}{S}$	total harmonic distortion-plus-noise to signal ratio	f_s = 44.1 kHz; R_L = 5 kΩ				
		at input signal of 1 kHz (0 dB)	–	–90[2]	–80	dB
			–	0.0032	0.01	%
		at input signal of 1 kHz (–60 dB)	–	–30[2]	–20	dB
			–	3.2	10	%
S/N_{bz}	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	90	95	–	dBA
$V_{o(FS)(rms)}$	full-scale output voltage (RMS value)	V_{DD} = 3.3 V	–	0.66	–	V
General characteristics						
$f_{i(sample)}$	audio sample input frequency		5	–	55	kHz
T_{amb}	operating ambient temperature		0	25	70	°C

Notes

1. V_{DD} is the supply voltage on pins V_{DDA}, V_{DDE}, V_{DDI} and V_{DDX}. V_{SS} is the ground on pins V_{SSA}, V_{SSE}, V_{SSI} and V_{SSX}. All V_{DD} and V_{SS} pins must be connected to the same supply or ground respectively.
2. The audio information from the USB interface is fed directly to the ADAC.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
UDA1331H	QFP64	plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 × 20 × 2.8 mm	SOT319-2

BLOCK DIAGRAM

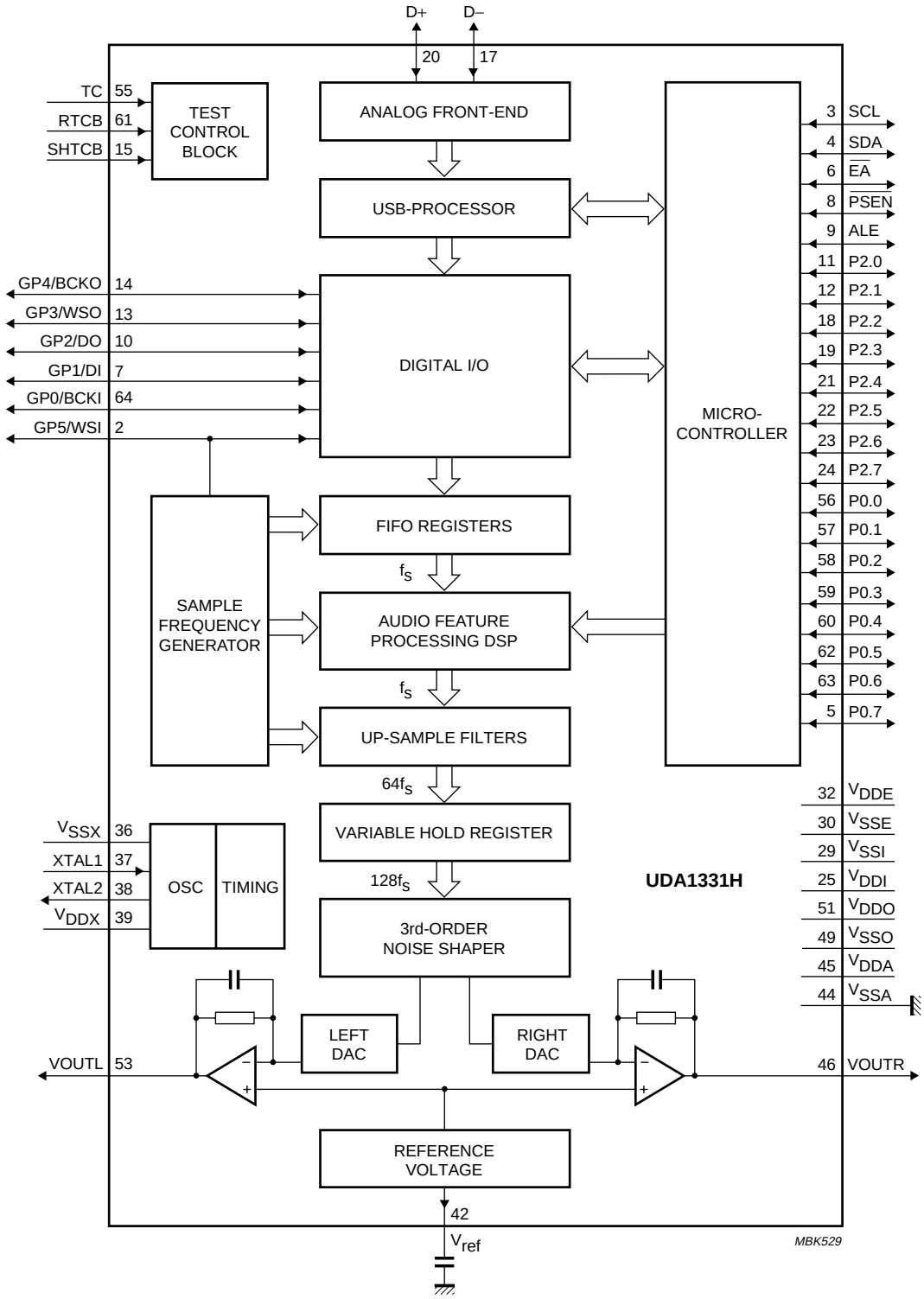


Fig.1 Block diagram.

PINNING

SYMBOL	PIN	I/O	DESCRIPTION
n.c.	1	–	not connected
GP5/WSI	2	I/O	general purpose pin 5 or word select input
SCL	3	I/O	serial clock input (I^2C-bus)
SDA	4	I/O	serial data input/output (I^2C-bus)
P0.7	5	I/O	Port 0.7 of the microcontroller
$\overline{EA}$	6	I/O	external access (active LOW)
GP1/DI	7	I/O	general purpose pin 1 or data input
$\overline{PSEN}$	8	I/O	program store enable (active LOW)
ALE	9	I/O	address latch enable (active HIGH)
GP2/DO	10	I/O	general purpose pin 2 or data output for extra DSP chip
P2.0	11	I/O	Port 2.0 of the microcontroller
P2.1	12	I/O	Port 2.1 of the microcontroller
GP3/WSO	13	I/O	general purpose pin 3 or master word select output for extra DSP chip
GP4/BCKO	14	I/O	general purpose pin 4 or master bit clock output for extra DSP chip
SHTCB	15	I	shift clock TCB input (active HIGH)
n.c.	16	–	not connected
D–	17	I/O	negative data line of the differential data bus conform to the USB-standard
P2.2	18	I/O	Port 2.2 of the microcontroller
P2.3	19	I/O	Port 2.3 of the microcontroller
D+	20	I/O	positive data line of the differential data bus conform to the USB-standard
P2.4	21	I/O	Port 2.4 of the microcontroller
P2.5	22	I/O	Port 2.5 of the microcontroller
P2.6	23	I/O	Port 2.6 of the microcontroller
P2.7	24	I/O	Port 2.7 of the microcontroller
V_{DDI}	25	–	digital supply voltage core
n.c.	26	–	not connected
n.c.	27	–	not connected
n.c.	28	–	not connected
V_{SSI}	29	–	digital ground core
V_{SSE}	30	–	digital ground I/O pins
n.c.	31	–	not connected
V_{DDE}	32	–	digital supply voltage I/O pins
n.c.	33	–	not connected
n.c.	34	–	not connected
n.c.	35	–	not connected
V_{SSX}	36	–	crystal oscillator ground
XTAL1	37	I	crystal oscillator input 1
XTAL2	38	O	crystal oscillator output 2
V_{DDX}	39	–	crystal oscillator supply voltage
n.c.	40	–	not connected

SYMBOL	PIN	I/O	DESCRIPTION
n.c.	41	–	not connected
V_{ref}	42	O	reference output voltage
n.c.	43	–	not connected
V_{SSA}	44	–	analog ground
V_{DDA}	45	–	analog supply voltage
VOUTR	46	O	right channel output voltage
n.c.	47	–	not connected
n.c.	48	–	not connected
V_{SSO}	49	–	operational amplifier ground
n.c.	50	–	not connected
V_{DDO}	51	–	operational amplifier supply voltage
n.c.	52	–	not connected
VOUTL	53	O	left channel output voltage
n.c.	54	–	not connected
TC	55	I	test control input (active HIGH)
P0.0	56	I/O	Port 0.0 of the microcontroller
P0.1	57	I/O	Port 0.1 of the microcontroller
P0.2	58	I/O	Port 0.2 of the microcontroller
P0.3	59	I/O	Port 0.3 of the microcontroller
P0.4	60	I/O	Port 0.4 of the microcontroller
RTCB	61	I	asynchronous reset input for test control box (active HIGH)
P0.5	62	I/O	Port 0.5 of the microcontroller
P0.6	63	I/O	Port 0.6 of the microcontroller
GP0/BCKI	64	I/O	general purpose pin 0 or master bit clock input

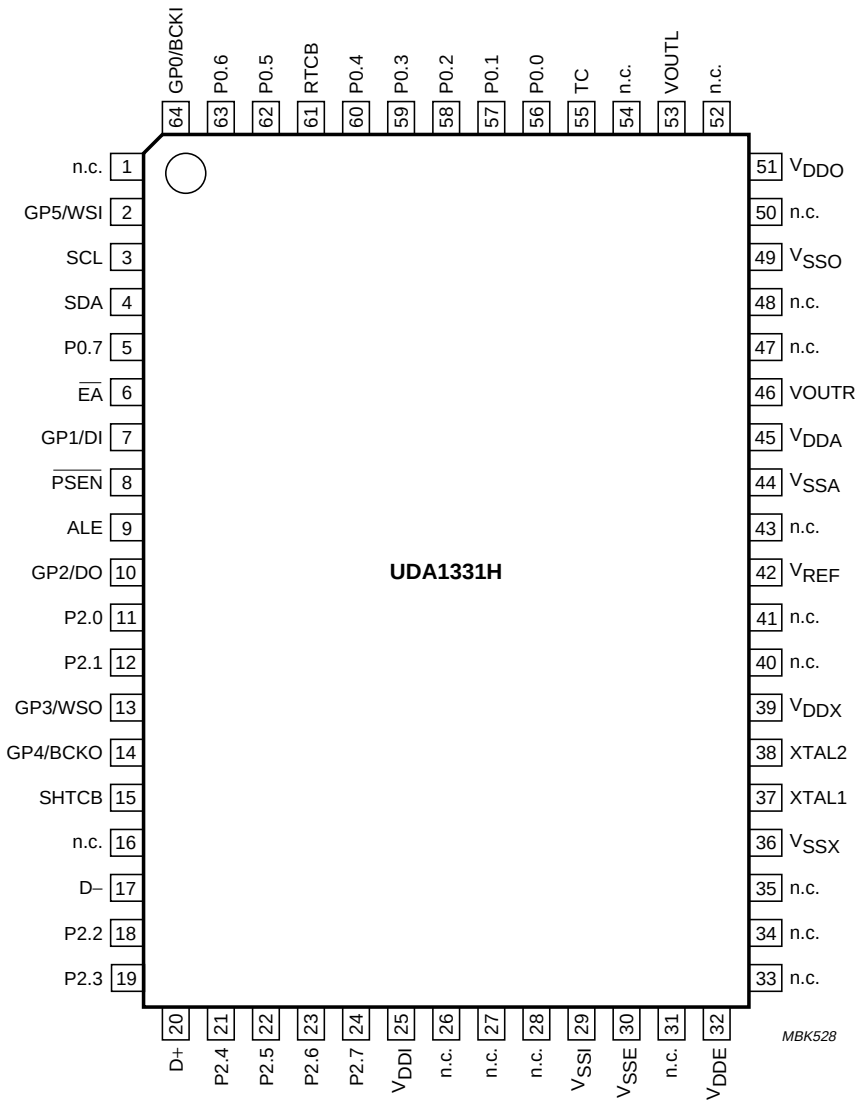


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

All bold-faced parameters given in this data sheet such as 'bAlternateSetting' are part of the USB specification as described in *"USB Device Class Definition for Audio Devices"*.

The Universal Serial Bus (USB)

Data and power are transferred via the USB by a 4-wire cable. The signalling occurs via two wires and point-to-point segments. The signals on each segment are differentially driven into a cable of 90 Ω intrinsic impedance. The differential receiver features input sensitivity of at least 200 mV and sufficient common mode rejection.

The analog front-end

The analog front-end is an on-chip generic USB transceiver. It is designed to allow voltage levels up to V_{DD} from standard or programmable logic to interface with the physical layer of the USB. It is capable of receiving and transmitting serial data at full speed (12 Mbits/s).

The USB processor

The USB processor forms the interface between the analog front-end, the ADAC and the microcontroller. The USB processor consists of:

- The Philips Serial Interface Engine (PSIE)
- The Memory Management Unit (MMU)
- The Audio Sample Redistribution (ASR) module.

The Philips Serial Interface Engine and Memory Management Unit (PSIE and MMU)

The PSIE and MMU translate the electrical USB signals into bytes and signals. Depending upon the USB device address and the USB endpoint address, the USB data is directed to the correct endpoint buffer on the PSIE and MMU interface. The data transfer could be of the bulk, isochronous, control or interrupt type. The USB device address is configured during the enumeration process. The UDA1331H has three endpoints. These are:

- Control endpoint 0
- Status interrupt endpoint
- Isochronous data sink endpoint.

The amount of bytes per packet on the control endpoint is limited by the PSIE and MMU hardware to 8 bytes per packet.

The PSIE is the digital front-end of the USB processor. This module recovers the 12 MHz USB clock, detects the USB sync word and handles all low-level USB protocols and error checking.

The MMU is the digital back-end of the USB processor. It handles the temporary data storage of all USB packets that are received or sent over the bus. Three types of packets are defined on the USB. These are:

- Token packets
- Data packets
- Handshake packets.

The token packet contains information about the destination of the data packet. The audio data is transferred via an isochronous data sink endpoint and consequently no handshaking mechanism is used. The MMU also generates a 1 kHz clock that is locked to the USB Start-Of-Frame (SOF) token.

The Audio Sample Redistribution (ASR) module

The ASR module reads the audio samples from the MMU and distributes these samples equidistant over a 1 ms frame period. The distributed audio samples are translated by the digital I/O module to standard I^2S-bus format or Japanese digital I/O format. The ASR module generates the bit clock and the word select signal of the digital I/O. The digital I/O formats the received audio samples to one of the four specified serial digital audio formats (standard I^2S-bus, 16, 18 or 20 bits LSB-justified).

The microcontroller

The microcontroller receives the control information selected from the USB by the USB processor. It handles the high-level USB protocols and the user interfaces.

The major task of the software process, that is mapped upon the microcontroller, is to control the different modules of the UDA1331H in such a way that it behaves as a USB device. Therefore the microcontroller:

- Interprets the USB requests and maps them upon the UDA1331H application
- Controls the internal operation of the UDA1331H and the digital I/O pins
- Communicates with the external world (EEPROM) using the I^2C-bus facility and the general purpose I/O pins.

The firmware must be located in an external (E)PROM. The UDA1331H will be delivered with standard USB compliant firmware.

The Asynchronous Digital-to-Analog Converter (ADAC)

The ADAC receives USB audio information from the USB processor or from the digital I/O-bus. The ADAC is able to reconstruct the sample clock from the rate at which the audio samples arrive and handles the audio sound processing. After processing, the audio signal is up-sampled, noise-shaped and converted to analog output voltages capable of driving a line output. The ADAC consists of:

- A Sample Frequency Generator (SFG)
- First-In First-Out (FIFO) registers
- An audio feature processing DSP
- Two digital up-sample filters
- A variable hold register
- A digital Noise Shaper (NS)
- A Filter Stream DAC (FSDAC) with integrated filter and line output drivers.

The Sample Frequency Generator (SFG)

The SFG controls the timing signals for the asynchronous digital-to-analog conversion. By means of a digital PLL, the SFG automatically recovers the applied sampling frequency and generates the accurate timing signals for the audio feature processing DSP and the up-sample filters.

First-In First-Out (FIFO) registers

The FIFO registers are used to store the audio samples temporarily coming from the USB processor or from the digital I/O input. The use of a FIFO register (in conjunction with the SFG) is necessary to remove all jitter present on the incoming audio signal.

The audio feature processing DSP

A DSP processes the sound features. The control and mapping of the sound features is explained in Section “Controlling the USB Audio Playback Peripheral (APP)”. Depending on the sampling rate (f_s) the DSP has four frequency domains in which the treble and bass are regulated (see Table 1). The domain is chosen automatically.

The up-sample filters and variable hold register

After the audio feature processing DSP two up-sample filters and a variable hold register increase the oversampling rate to $128f_s$.

Table 1 Frequency domains for audio processing

DOMAIN	SAMPLE FREQUENCY (kHz)
1	5 to 12
2	12 to 25
3	25 to 40
4	40 to 55

The noise shaper

A 3rd-order noise shaper converts the oversampled data to a noise-shaped bitstream for the FSDAC. The in-band quantization noise is shifted to frequencies well above the audio band.

The Filter Stream DAC (FSDAC)

The FSDAC is a semi-digital reconstruction filter that converts the 1-bit data stream of the noise shaper to an analog output voltage. The filter coefficients are implemented as current sources and are summed at virtual ground of the output operational amplifier. In this way very high signal-to-noise performance and low clock jitter sensitivity is achieved. A post filter is not needed because of the inherent filter function of the DAC. On-board amplifiers convert the FSDAC output current to an output voltage signal capable of driving a line output.

USB Audio Playback Peripheral (APP) descriptors

In a typical USB environment the USB host has to know which kind of devices are connected. For this purpose each device contains a number of USB descriptors. These descriptors describe, from different points of view (USB configuration, USB interface and USB endpoint), the capabilities of a device. Each of them can be requested by the host. The collection of descriptors is denoted as a descriptor map. This descriptor map will be reported to the USB host during enumeration and on request.

The full descriptor map is implemented in the firmware exploiting the full functionality of the UDA1331H. The USB descriptors and their most important fields, in relationship to the characteristics of the UDA1331H are briefly explained below.

General descriptors

The UDA1331H supports one configuration containing a control interface, an audio interface and a HID interface. The descriptor map that describes this configuration is partly fixed and partly programmable.

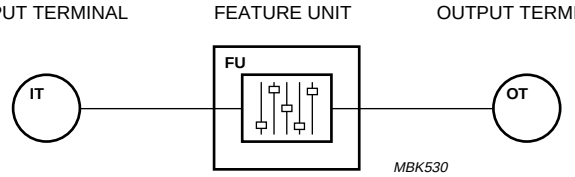


Fig.3 Audio function topology.

The programmable part can be retrieved from one of four configuration maps located in the (E)PROM or from an I²C-bus EEPROM. At start-up one of four configuration maps can be selected depending on the logical combination of GP3 and GP0. It is possible to overwrite this configuration map with a configuration map loaded from an I²C-bus EEPROM.

AUDIO DEVICE CLASS SPECIFIC DESCRIPTORS

The audio device class is partly specified with standard descriptors and partly with specific audio device class descriptors. The standard descriptors specify the number and the type of the interface or endpoint. The UDA1331H supports 7 different audio modes:

- 8-bit Pulse Code Modulation (PCM) mono or stereo audio data
- 16-bit PCM mono or stereo audio data
- 24-bit PCM mono or stereo audio data
- Zero bandwidth mode.

Each mode is defined as an alternate setting of the audio interface, selectable with the standard audio streaming interface descriptor **bAlternateSetting** field.

The seven alternate settings are described in more detail by the specific audio device class descriptors.

The UDA1331H supports the Input Terminal (IT), Output Terminal (OT) and the Feature Unit (FU) descriptors.

The input and output terminals are not controllable via the USB. The feature unit provides the basic manipulation of the incoming logical channels.

The supported sound features are:

- Volume control
- Mute control
- Treble control
- Bass control
- Bass boost control.

Table 2 Audio bandwidth at each audio mode

AUDIO MODE	wMaxPacketSize
8-bit PCM; mono	56 ($^{8}/_{8} \times 1 \times 56$)
8-bit PCM; stereo	112 ($^{8}/_{8} \times 2 \times 56$)
16-bit PCM; mono	112 ($^{16}/_{8} \times 1 \times 56$)
16-bit PCM; stereo	224 ($^{16}/_{8} \times 2 \times 56$)
24-bit PCM; mono	168 ($^{24}/_{8} \times 1 \times 56$)
24-bit PCM; stereo	336 ($^{24}/_{8} \times 2 \times 56$)

The maximum number of audio data samples within a USB packet arriving on the isochronous sink endpoint is restricted by the buffer capacity of this isochronous endpoint. The maximum buffer capacity is 336 bytes/ms.

For each alternate setting with audio, a maximum bandwidth is claimed as indicated in the standard isochronous audio data endpoint descriptor **wMaxPacketSize** field. To allow a small overshoot in the number of audio samples per packet, the top sample frequency of 55 kHz is taken in the calculation of the bandwidth for each alternate setting. For each alternate setting, with its own isochronous audio data endpoint descriptor, **wMaxPacketSize** field is then defined as described in Table 2.

Although in a specific UDA1331H application no endpoint control properties can be used upon the isochronous adaptive sink endpoint, the descriptors are still necessary to inform the host about the definition of this endpoint: isochronous, adaptive, sink, continuous sampling frequency (at input side of this endpoint) with lower bound of 5 kHz and upper bound of 55 kHz.

The audio class specific descriptors can be requested with the ‘Get descriptor: configuration request’, which returns all the descriptors, except the device descriptor.

HUMAN INTERFACE DEVICE SPECIFIC DESCRIPTORS

The inputs defined on the UDA1331H are transmitted via the USB to the host according to the HID class. The host responds with the appropriate settings via the audio device class for the audio related parts or via the HID class for the HID related inputs and outputs of the UDA1331H.

A HID descriptor is necessary to inform the host about the conception of the user interface. The host communicates via the HID device driver using either the control pipe or the interrupt pipe. The UDA1331H uses USB endpoint 0 (control pipe) to respond to the HID specific 'Get/set report request' to receive or transmit data from or to the UDA1331H. The UDA1331H uses the status interrupt endpoint as interrupt pipe for polling asynchronous data.

The UDA1331H is a high-speed device. The maximum transaction size is 64 bytes per USB frame and the polling rate is defined at a maximum of every 1 ms.

The host requests the configuration descriptor which includes the standard interface descriptor, the HID endpoint descriptor and the HID descriptor. The HID device driver of the host then requests the report descriptor.

Report descriptors are composed of pieces of information about the device. Each piece of information is called an item. All items have a 1-byte prefix that contains the item tag, type and size. In the UDA1331H only the short item basic type is used.

The hosts HID device driver will parse the report descriptor and the defined items. By examining all of these items, the HID class driver is able to determine the size and composition of data reports from the device.

The main items of the UDA1331H are input and output reports. Input reports are sent via the interrupt pipe (UDA1331H USB address 3). Input and output reports can be requested by the host via the control endpoint (USB address 0).

The UDA1331H supports a maximum of three pushbuttons, which represents a certain feature of the UDA1331H. If pressed by the user the pushbutton will go to its 'ON' state, if not pressed the pushbutton will go back to its 'OFF' state. The UDA1331H supports a maximum of two outputs for e.g. user LEDs.

For more information about the input and output functions of the UDA1331H see the application documentation of the device.

Controlling the USB Audio Playback Peripheral (APP)

This section describes the functionality of the feature unit of the UDA1331H. The mapping of this functionality onto USB descriptors is as implemented in the firmware.

The sound features as defined in the *"USB Device Class Definition for Audio Devices"* are mapped on the UDA1331H specific feature registers by the microcontroller. These specific sound features are:

- Volume control (separate for left and right stereo channels, no master channel)
- Mute control (only master channel)
- Treble control (only master channel)
- Bass control (only master channel)
- Dynamic bass boost control (only master channel).

These specific features can be activated via the host (audio device class requests) or via the GP pins (HID plus audio device class requests). Via the I^2C-bus the user is able to download the necessary configuration data for different applications (definition of the function of the GP pins, with or without digital I/O functionality, etc.).
The mapping and control of the standard USB audio features and UDA1331H specific features is described below.

VOLUME CONTROL

Volume control is possible via the host or via predefined GP pins. The setting of 0 dB is always referenced to the maximum available volume setting. Table 3 gives the mapping of **wVolume** value (as defined in the *"USB Device Class Definition for Audio Devices"*) upon the actual volume setting of the USB APP. When using the UDA1331H, the range is 0 down to −60 dB (in steps of 1 dB) and −∞ dB. Independant control of 'left'/'right' volume is possible. It should be noted that **wVolume** bits B7 to B0 are not used. Values above 0 dB are returned as 0 dB. The volume value at start-up of the device is defined in the selected configuration map.

Balance control is possible via the separate volume control option of both channels. Therefore the characteristics of the balance control are equal to the volume control characteristics.

Table 3 Volume control characteristics

wVOLUME								VOLUME USB SIDE (dB)	VOLUME USB APP (dB)
B15	**B14**	**B13**	**B12**	**B11**	**B10**	**B9**	**B8**		
0	0	0	0	0	0	0	0	0	0
1	1	1	1	1	1	1	1	–1	–1
1	1	1	1	1	1	1	0	–2	–2
1	1	1	1	1	1	0	1	–3	–3
1	1	1	1	1	1	0	0	–4	–4
1	1	1	1	1	0	1	1	–5	–5
1	1	1	1	1	0	1	0	–6	–6
1	1	1	1	1	0	0	1	–7	–7
1	1	1	1	1	0	0	0	–8	–8
1	1	1	1	0	1	1	1	–9	–9
1	1	1	1	0	1	1	0	–10	–10
...	...	...	...	...	...	...	...	...	...
1	1	0	0	0	1	0	1	–59	–59
1	1	0	0	0	1	0	0	–60	–60
1	1	0	0	0	0	1	1	–61	–∞
1	1	0	0	0	0	1	0	–62	–∞
...	...	...	...	...	...	...	...	...	...
1	0	0	0	0	0	0	0	–∞	–∞

MUTE CONTROL

Mute is one of the sound features as defined in the *"USB Device Class Definition for Audio Devices"*. The mute control request data **bMute** controls the position of the mute switch. The position can be either on or off. When **bMute** is true the feature unit is muted. When **bMute** is false the feature unit is not muted.

When the mute is active for the master channel, the value of the sample is decreased smoothly to zero following a raised cosine curve. There are 32 coefficients used to step down the value of the data, each one being used 32 times before stepping to the next.

This amounts to a mute transition of 23 ms at f_s = 44.1 kHz. When the mute is released, the samples are returned to the full level again following a raised cosine curve with the same coefficients being used in reversed order. The mute, on the master channel is synchronized to the sample clock, so that operation always takes place on complete samples.

A mute can be given via the host or by pressing a predefined GP pin.

TREBLE CONTROL

The treble control is available for the master channel of the UDA1331H. Treble can be regulated in three modes: minimum, flat and maximum mode. The preferred mode is selected at start-up of the device (configuration map). The corner frequency is 3000 Hz for the minimum mode and 1500 Hz for the maximum mode. The treble range is from 0 to 6 dB in steps of 2 dB. It should be noted that the negative treble values as defined in the *"USB Device Class Definition for Audio Devices"* are not supported by the UDA1331H; the 0 dB value is returned as 0 dB. Table 4 gives the mapping of the **bTreble** value upon the actual treble setting of the USB APP.

Table 4 Treble control characteristics

bTREBLE								TREBLE USB SIDE (dB)	TREBLE USB APP (dB)		
B7	B6	B5	B4	B3	B2	B1	B0		minimum	flat	maximum
0	0	0	0	0	0	0	0	0.00	0	0	0
0	0	0	0	0	0	0	1	0.25			
0	0	0	0	0	0	1	0	0.50			
0	0	0	0	0	0	1	1	0.75			
0	0	0	0	0	1	0	0	1.00			
0	0	0	0	0	1	0	1	1.25	2	0	2
0	0	0	0	0	1	1	0	1.50			
0	0	0	0	0	1	1	1	1.75			
0	0	0	0	1	0	0	0	2.00			
0	0	0	0	1	0	0	1	2.25			
0	0	0	0	1	0	1	0	2.50			
0	0	0	0	1	0	1	1	2.75			
0	0	0	0	1	1	0	0	3.00			
0	0	0	0	1	1	0	1	3.25	4	0	4
								...			
0	0	0	1	0	1	0	1	5.25	6	0	6
								...			
0	0	0	1	1	1	0	1	7.25	6	0	6
								...			
0	0	1	0	0	1	0	1	9.25	6	0	6
								...			
0	1	1	1	1	1	1	1	31.75	6	0	6

BASS CONTROL

The bass control is available for the master channel of the UDA1331H. Bass can be regulated in three modes: minimum, flat and maximum mode. The preferred mode is selected at start-up of the device (configuration map). The Bass range is from 0 to about 14 dB (minimum mode) or about 24 dB (maximum mode) in steps of 2 dB. It should be noted that the negative bass values as defined in the *"USB Device Class Definition for Audio Devices"* are not supported by the UDA1331H; the 0 dB value is returned as 0 dB. The maximum Bass value which will be reported to the host is always 24 dB independent of the mode. The maximum mode is the most accurate mode when the Bass values are reported to the host. The corner frequency is 100 Hz for the minimum mode and 75 Hz for the maximum mode. Table 5 gives the mapping of the **bBass** value upon the actual bass setting of the USB APP.

Table 5 Bass control characteristics

bBASS								BASS USB SIDE (dB)	BASS USB APP (dB)		
B7	B6	B5	B4	B3	B2	B1	B0		minimum	flat	maximum
0	0	0	0	0	0	0	0	0.00	0	0	0
0	0	0	0	0	0	0	1	0.25			
0	0	0	0	0	0	1	0	0.50			
0	0	0	0	0	0	1	1	0.75			
0	0	0	0	0	1	0	0	1.00			
0	0	0	0	0	1	0	1	1.25	1.1	0	1.7
0	0	0	0	0	1	1	0	1.50			
0	0	0	0	0	1	1	1	1.75			
0	0	0	0	1	0	0	0	2.00			
0	0	0	0	1	0	0	1	2.25			
0	0	0	0	1	0	1	0	2.50			
0	0	0	0	1	0	1	1	2.75			
0	0	0	0	1	1	0	0	3.00			
0	0	0	0	1	1	0	1	3.25	2.4	0	3.6
								...			
0	0	0	1	0	1	0	1	5.25	3.7	0	5.4
								...			
0	0	0	1	1	1	0	1	7.25	5.2	0	7.4
								...			
0	0	1	0	0	1	0	1	9.25	6.8	0	9.4
								...			
0	0	1	0	1	1	0	1	11.25	8.4	0	11.3
								...			
0	0	1	1	0	1	0	1	13.25	10.2	0	13.3
								...			
0	0	1	1	1	1	0	1	15.25	11.9	0	15.2
								...			
0	1	0	0	0	1	0	1	17.25	13.7	0	17.3
								...			

bBASS								BASS USB SIDE (dB)	BASS USB APP (dB)		
B7	B6	B5	B4	B3	B2	B1	B0		minimum	flat	maximum
0	1	0	0	1	1	0	1	19.25	13.7	0	19.2
								...			
0	0	1	1	1	0	1	1	21.25	13.7	0	21.2
								...			
0	1	0	1	0	1	0	1	23.25	13.7	0	23.2
								...			
0	1	1	0	0	1	0	1	25.25	13.7	0	23.2
								...			
0	1	1	0	1	1	0	1	27.25	13.7	0	23.2
								...			
0	1	1	1	0	1	0	1	29.25	13.7	0	23.2
								...			
0	1	1	1	1	1	0	1	31.25	13.7	0	23.2
								...			
0	1	1	1	1	1	1	1	31.75	13.7	0	23.2

DYNAMIC BASS BOOST CONTROL

Bass boost is one of the sound features as defined in the *"USB Device Class Definition for Audio Devices"*.
The bass boost control request data **bBassBoost** controls the position of the bass boost switch. The position can be either on or off. When **bBassBoost** is true the bass boost is activated. When **bBassBoost** is false the bass boost is off.

When clipping prevention is active, the bass is reduced to avoid clipping with high volume settings. Bass boost is selectable via the configuration map (see Table 6).
If byte 19H is loaded with 00H, bass boost is not reported to the USB host by the device.

Clipping prevention

If the maximum of the bass plus volume gives clipping, the Bass is reduced. Clipping prevention is selectable via the configuration map.

De-emphasis

De-emphasis is one of the properties which is not supported by the USB. De-emphasis for 44.1 kHz can be predefined in the configuration map selected at start-up of the UDA1331H.

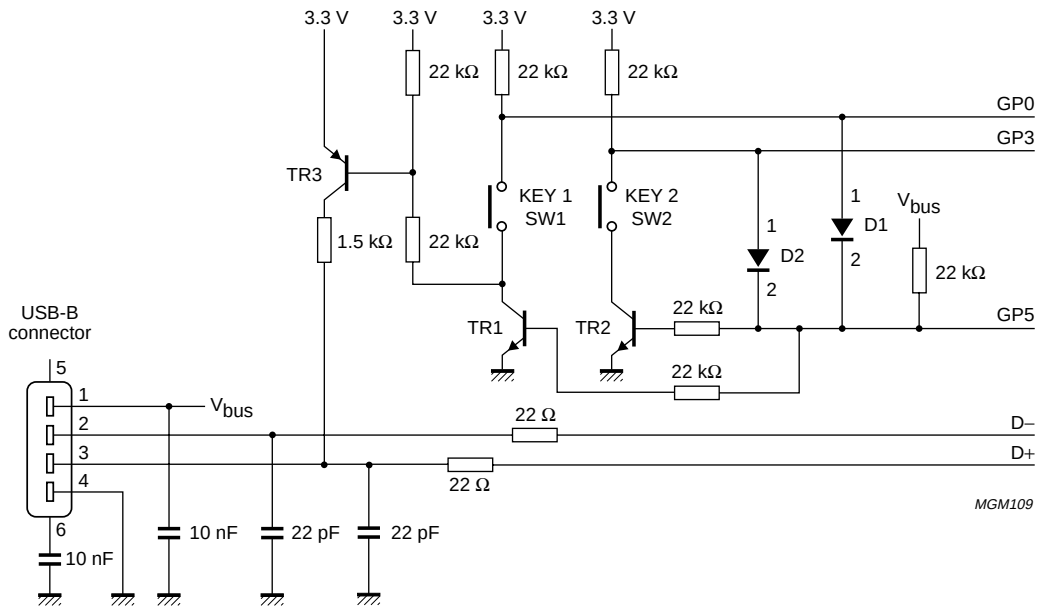


Fig.4 Diode matrix selection.

Start-up and configuration of the UDA1331H

START-UP OF THE UDA1331H

After power-on, an internal power-on reset signal becomes HIGH after a certain RC-time (R = 5 kΩ and C = C_{ref}). During 10 ms after power-on reset the UDA1331H has to initiate the internal settings. After the power-on reset the UDA1331H becomes master of the I²C-bus.
The UDA1331H tries to read the eventually connected EEPROM and if an EEPROM is detected, the internal descriptors are overwritten and the selected port configuration is applied. If no EEPROM is detected, the UDA1331H tries to read the logical levels of GP3 and GP0. A choice can be made from four configuration maps via these two pins.

CONFIGURATION SELECTION OF THE UDA1331H VIA A DIODE MATRIX

The UDA1331H uses a configuration map to hold a number of specific configurable data on hardware, product, component and USB configuration level.
At start-up without EEPROM, the UDA1331H will scan the logical levels of GP3 and GP0. With these two pins it is possible to select one of the four possible (vendor specific) configuration maps which are held in the external (E)PROM. This selection can be achieved via a diode matrix (see Fig.4).

After selecting a configuration map the user cannot change the chosen settings for the GP pins, internal configuration, descriptors, etc.

For more information about the four (vendor specific) configuration maps located in the (E)PROM and the diode matrix see the application documentation.

CONFIGURATION OPTIONS OF THE UDA1331H VIA AN I²C-BUS EEPROM

If an EEPROM is detected (reading byte 0 as AAH and byte 1 as 55H), the UDA1331H will use the configuration map in the EEPROM instead of one of four configuration maps. The layout of the configuration map is fixed, the values (except bytes 0 and 1) are user definable (see Table 6). If the user wants to change these values (the manufacturers name for instance), this can be achieved via the EEPROM code.

The communication between the UDA1331H and the external I²C-bus device is based on the standard I²C-bus protocol given in the Philips specification *"The I²C-bus and how to use it (including specifications)"*, which can be ordered using the code 9398 393 40011. The I²C-bus has two lines: a clock line SCL and a serial data line SDA (see Fig.5).

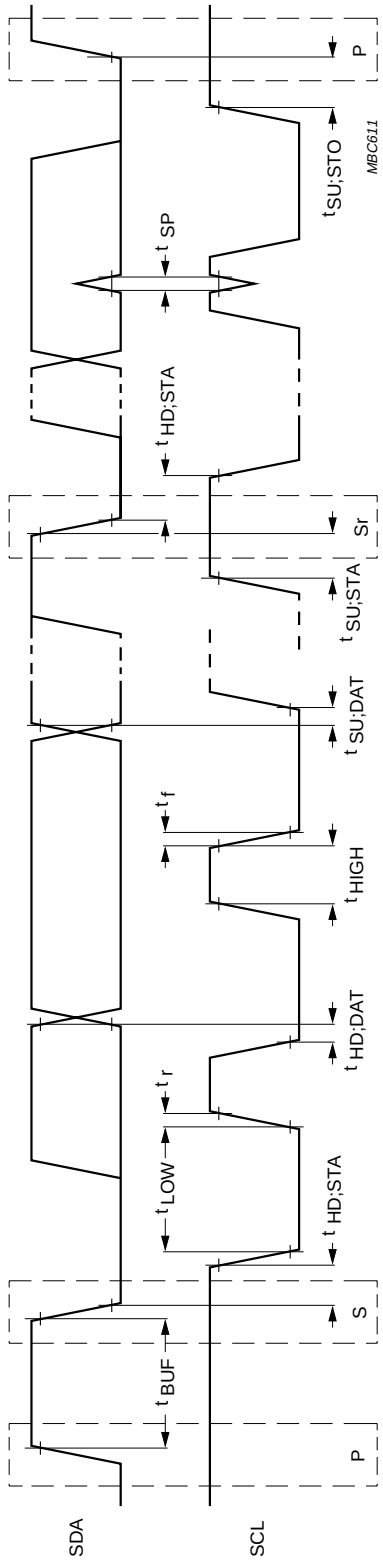


Fig.5 Definition of timing of the I²C-bus.

Table 6 Control options for the UDA1331H via the EEPROM configuration map; note 1

BYTE (HEX)	REGISTER NAME	COMMENTS	BIT	VALUE
0	–	recognition pattern; do not change it		AAH
1	–	recognition pattern; do not change it		55H
2	ASR control register	robust word clock	7	0 = off 1 = on
		serial I^2S-bus output format	6 and 5	00 = I^2S-bus 01 = 16-bit LSB 10 = 18-bit LSB 11 = 20-bit LSB
		phase inversion	4	0 = mono phase inversion off 1 = mono phase inversion on
		bits per sample modi	3 and 2	00 = reserved 01 = 8-bit audio 10 = 16-bit audio 11 = 24-bit audio
		audio mode	1	0 = mono 1 = stereo
		ASR register start-up mode	0	0 = stop 1 = go
3	ADAC mode register 0	selection ADAC mode register	7	0
		audio feature mode	6 and 5	00 = flat 01 = minimum 10 = minimum 11 = maximum
		de-emphasis	4	0 = de-emphasis off 1 = de-emphasis on
		channel manipulation	3	0 = L $\Rightarrow$ L, R $\Rightarrow$ R 1 = L $\Rightarrow$ R, R $\Rightarrow$ L
		synchronous/asynchronous control	2	0 = asynchronous 1 = synchronous
		mute control	1	0 = no mute 1 = mute active
		reset ADAC	0	0 = no reset ADAC 1 = reset ADAC

BYTE (HEX)	REGISTER NAME	COMMENTS	BIT	VALUE
4	ADAC mode register 1	selection ADAC mode register	7	1
		digital PLL lock speed	6 and 5	00 = lock after 512 samples 01 = lock after 2048 samples 10 = lock after 4096 samples 11 = lock after 16384 samples
		digital PLL lock mode	4	0 = adaptive 1 = fixed
		digital PLL mode	3 and 2	00 = adaptive 01 = fixed state 1 10 = fixed state 2 11 = fixed state 3
		serial I^2S-bus input format	1 and 0	00 = I^2S-bus 01 = 16-bit LSB 10 = 18-bit LSB 11 = 20-bit LSB
5	I/O selection register	clipping	7	0 = clipping prevention off 1 = clipping prevention on
		I^2S-bus usage	6	0 = no I^2S-bus used 1 = I^2S-bus used
		4/6 pins I^2S-bus (see Section “The general purpose pins (GP0 to GP5)”)	5	only if I^2S-bus is used; 0 = 4 pins I^2S-bus 1 = 6 pins I^2S-bus
		GP4	4	0 = function 1 1 = function 2 (see Tables 7, 8 and 9)
		GP3	3	
		GP2	2	
		GP1	1	
		GP0	0	
6		GP0 Usage Page if HID selected		
7		GP0 Usage if HID selected		
8		reserved		
9		reserved		
A		GP3 Usage Page if HID selected		
B		GP3 Usage if HID selected		
C		reserved		
D		reserved		
E		GP4 Usage Page if HID selected		
F		GP4 Usage if HID selected		
10		reserved		

BYTE (HEX)	REGISTER NAME	COMMENTS	BIT	VALUE
11	GP1 and GP2 outputs definition register	reserved	7	
		reserved	6	
		application GP2 function 2	5	0 = HID output 2 1 = LED output 2 (activated when DBB is active)
		application GP1 function 2	4	0 = HID output 1 1 = LED output 1 (activated when mute is active)
		polarity GP2 function 1	3	normal or inversed output functionality: 0 = according Table 7 1 = inversed
		polarity GP1 function 1	2	
		polarity GP2 function 2	1	
		polarity GP1 function 2	0	
12		GP1 Usage Page if HID selected		
13		GP1 Usage if HID selected		
14		GP2 Usage Page if HID selected		
15		GP2 Usage if HID selected		
16		time between releasing standby and enabling the audio output; steps of 20 ms		
17		time between ‘no isochronous data present’ and activating the mute output; steps of 1 s; (only applicable for function 1; no digital I/O communication)		
18		time between activating the mute output and activating the standby output; steps of 5 s; (only applicable for function 1; no digital I/O communication). When filled with zero standby will not be activated.		
19		default bass boost value on top of Bass USB APP for Dynamic Bass Boost (DBB); see Table 5		bass boost = register value; if bass boost + Bass USB APP is larger then the maximum value of Table 5, the maximum value is used (no bass boost in flat mode)
1A		default volume value of USB APP		volume = –register value
1B		**idVendor** high byte		
1C		**idVendor** low byte		
1D		**idProduct** high byte		
1E		**idProduct** low byte		
1F		**bmAttributes**		
20		maximum power steps of 2 mA with maximum 500 mA		

BYTE (HEX)	REGISTER NAME	COMMENTS	BIT	VALUE
21		**wTerminalType** high byte		
22		**wTerminalType** low byte		
23				
24				
25		pointer language string		32
26		pointer manufacturer string		36
27		pointer product string		46
28		pointer serial number		54
32 ⇒		language string		
36 ⇒	–	manufacturer string		
46 ⇒	–	product string		
54 ⇒	–	serial number; note 2		

Notes

1. An extensive description of the USB control options is available in the *"USB Device Class Definition for Audio Devices"*.
2. The serial number is only supported in the external configuration map and not in the four internal configuration maps.

The general purpose pins (GP0 to GP5)

The UDA1331H has 6 General Purpose (GP) pins; these are pins GP0 to GP5. These can be used either for digital I/O functions or for general purposes. The configurations presented are as implemented in the standard firmware.

There are basically three port configurations:

- No digital I/O communication
- 4-pins digital I/O communication
- 6-pins digital I/O communication.

These port configurations can be selected via the configuration map at start-up of the UDA1331H.

The user can make a selection between two functions for each of the pins GP0 to GP4 (see byte 5 in Table 6), except if digital I/O communication is selected (see Tables 7, 8 and 9).

Table 7 No digital I/O communication

PIN	INPUT/OUTPUT	FUNCTION 1	FUNCTION 2
GP5	output; not programmable; note 2	connect/disconnect	connect/disconnect
GP4	inputs; programmable; note 1	alarm mute; note 3	HID input 3
GP3		HID input 2	HID input 2
GP0		HID input 1	HID input 1
GP2	outputs; programmable	standby; note 4	HID/LED output 2; note 6
GP1		mute; note 5	HID/LED output 1; note 6

Notes

1. The input pins must have a pull-up resistor.
2. Connect/disconnect: holds the USB ‘disconnected’ as long as the initialization is not finished.
3. Alarm mute: input to switch the sound off; specially used if the USB host program does not respond to the control. This pin acts directly on the sound and passes the mute to the USB host.
4. Standby is switched on (output becomes LOW) after a programmable time if the mute is active (see Byte 18 in Table 6).
5. Mute is switched on (output becomes LOW) after a programmable time if the isochronous data flow is interrupted (see Byte 17 in Table 6).
6. For selection between HID/LED application see configuration map byte 11 (output is active HIGH).

Table 8 4-pins digital I/O communication

PIN	INPUT/OUTPUT	FUNCTION 1	FUNCTION 2
GP5	output; not programmable; note 1	connect/disconnect	connect/disconnect
GP4	digital I/O-bus	BCKO	BCKO
GP3		WSO	WSO
GP2		DO	DO
GP1		DI	DI
GP0	input; programmable	HID input 1	alarm mute; note 2

Notes

1. Connect/disconnect: holds the USB ‘disconnected’ as long as the initialization is not finished.
2. Alarm mute: input to switch the sound off; specially used if the USB host program does not respond to the control. This pin acts directly on the sound and passes the mute to the USB host.

Table 9 6-pins digital I/O communication

PIN	INPUT/OUTPUT	FUNCTION
GP5	digital I/O-bus	WSI
GP4		BCKO
GP3		WSO
GP2		DO
GP1		DI
GP0		BCKI

Filter characteristics

The overall filter characteristic of the UDA1331H in flat mode is given in Fig.6. The overall filter characteristic of the UDA1331H includes the filter characteristics of the DSP in flat mode plus the filter characteristic of the FSDAC (f_s = 44.1 kHz).

DSP extension port

An external DSP can be used for adding extra sound processing features via the digital I/O-bus. The UDA1331H supports the standard I^2S-bus data protocol and the LSB-justified serial data input format with word lengths of 16, 18 and 20 bits. Using the 4-pins digital I/O-bus the UDA1331H device acts as a master, controlling the BCK and WS signals. The period of the WS signal is determined by the number of samples in the 1 ms frame of the USB. This implies that the WS signal does not have a constant period time, but is jittery. Using the 6-pins digital I/O-bus GP2, GP3 and GP4 are the output pins (master) and GP0, GP1 and GP5 are the input pins (slave).

For characteristic timing of the I^2S-bus input interface see Figs 7 and 8.

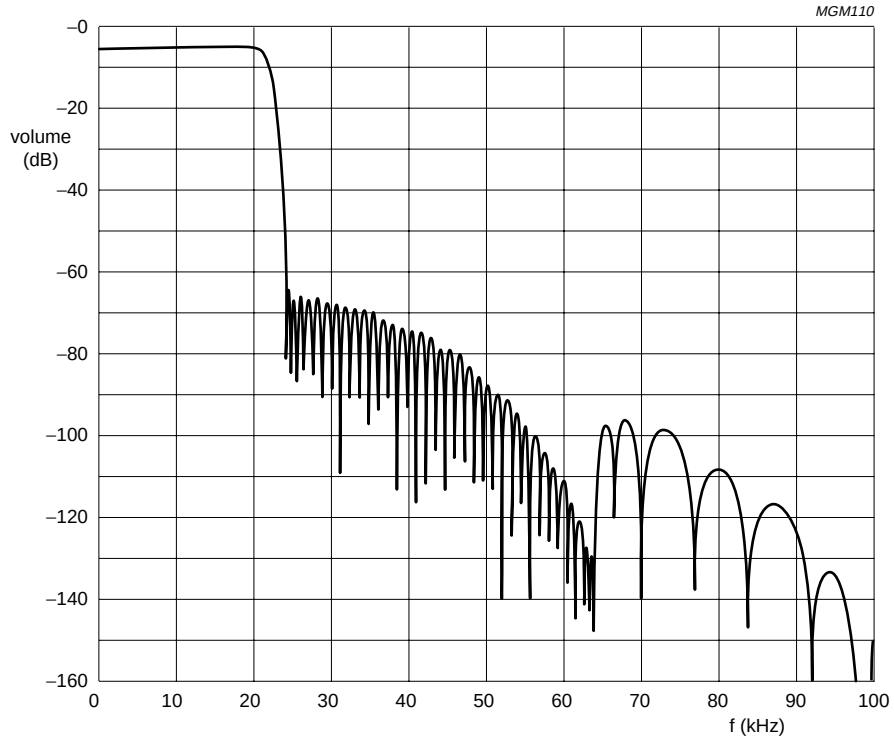


Fig.6 Overall filter characteristics of the UDA1331H.

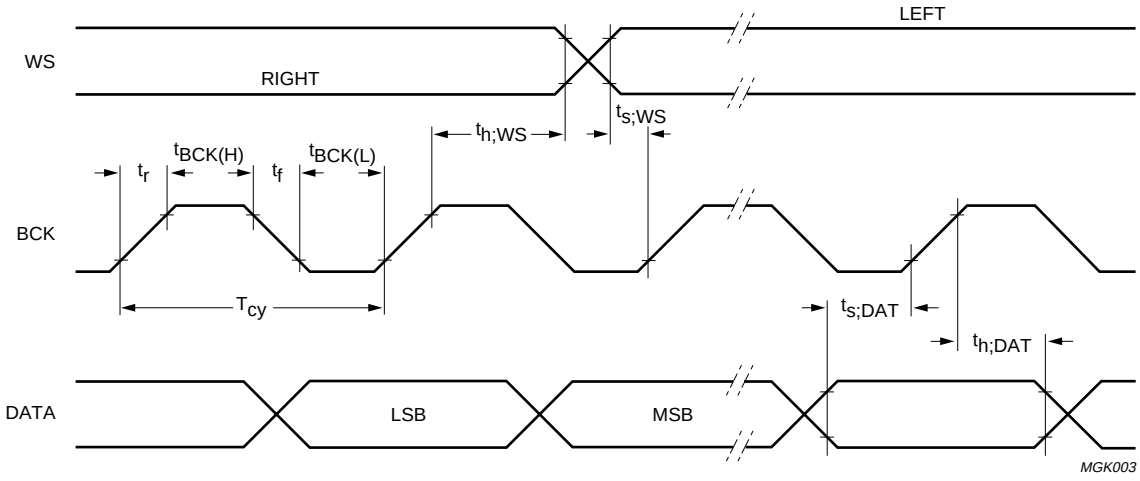


Fig.7 Timing of digital I/O input signals.

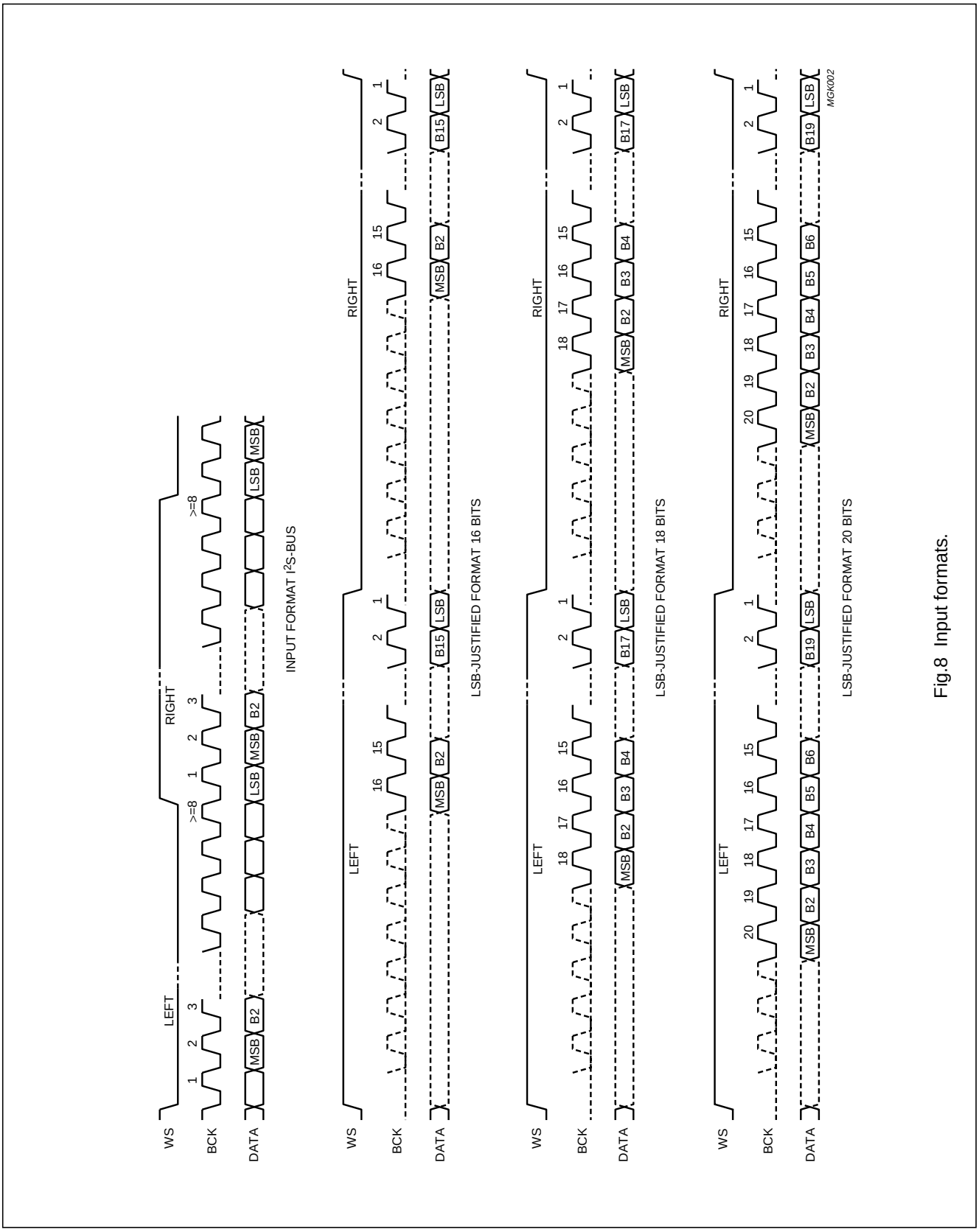


Fig.8 Input formats.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
All digital I/Os						
$V_{I/O}$	DC input/output voltage range		–0.5	–	V_{DD}	V
I_O	output current		–	–	4	mA
Temperature						
T_j	junction temperature		0	–	125	°C
T_{stg}	storage temperature		–55	–	+150	°C
T_{amb}	operating ambient temperature		0	25	70	°C
Electrostatic handling						
V_{es}	electrostatic handling	note 1	–3000	–	+3000	V
		note 2	–300	–	+300	V

Notes

1. Equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.
2. Equivalent to discharging a 200 pF capacitor through a 2.5 μH series inductor and a 25 Ω resistor.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	48	K/W

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{DD}	supply voltage	3.0	3.3	3.6	V
V_I	DC input voltage for D+ and D–	0.0	–	V_{DD}	V
$V_{I/O}$	DC input voltage for the digital I/Os	0.0	–	V_{DD}	V

DC CHARACTERISTICS

V_{DD} = 3.3 V; V_{SS} = 0 V; T_{amb} = 25 °C; f_{osc} = 48 MHz; f_s = 44.1 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supplies						
V_{DDE}	digital supply voltage I/O pins		3.0	3.3	3.6	V
V_{DDI}	digital supply voltage core		3.0	3.3	3.6	V
V_{DDA}	analog supply voltage		3.0	3.3	3.6	V
V_{DDO}	operational amplifier supply voltage		3.0	3.3	3.6	V
V_{DDX}	crystal oscillator supply voltage		3.0	3.3	3.6	V
I_{DDE}	digital supply current I/O pins	note 1	–	3	–	mA
I_{DDI}	digital supply current core		–	36	–	mA
I_{DDA}	analog supply current		–	4.2	–	mA
I_{DDO}	operational amplifier supply current		–	4.0	–	mA
I_{DDX}	crystal oscillator supply current		–	2.1	15.0[2]	mA
P_{tot}	total power dissipation		–	165	–	mW
$P_{tot(ps)}$	total power dissipation in power-save mode		–	60	–	mW
Inputs/outputs D+ and D–						
V_I	static DC input voltage		–0.5	–	V_{DDI}	V
V_{OH}	static DC output voltage HIGH	R_L = 15 kΩ to ground	2.8	–	V_{DDI}	V
V_{OL}	static DC output voltage LOW	R_L = 1.5 kΩ to 3.6 V	–	–	0.3	V
$\lvert I_{LO} \rvert$	high impedance state data line output leakage current		–	–	10	μA
$\Delta V_{I(dif)}$	differential input sensitivity		0.2	–	–	V
$V_{CM(dif)}$	differential common mode voltage		0.8	–	2.5	V
$V_{SE(RX)th}$	single-ended receiver threshold voltage		0.8	–	2.0	V
$C_{I(TRX)}$	transceiver input capacitance	pin to ground	–	–	20	pF
Digital inputs/outputs						
V_{IL}	LOW-level input voltage		–	–	$0.3V_{DDI}$	V
V_{IH}	HIGH-level input voltage		$0.7V_{DDI}$	–	V_{DDI}	V
V_{OL}	LOW-level output voltage		–	–	0.4	V
V_{OH}	HIGH-level output voltage		V_{DDI} – 0.4	–	–	V
$\lvert I_{LI} \rvert$	input leakage current		–	–	1	μA
C_i	input capacitance	pin to ground	–	–	5	pF

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Filter stream DAC						
V_{ref}	reference voltage		–	$0.5V_{DDA}$	–	V
$V_{o(cm)}$	common mode output voltage		–	$0.5V_{DDA}$	–	V
R_o	output resistance at pins VOUTL and VOUTR		–	11	–	Ω
$R_{o(L)}$	output load resistance		2.0	–	–	kΩ
$C_{o(L)}$	output load capacitance		–	–	50	pF

Notes

1. This value depends strongly on the application. The specified value is the typical value obtained using the application as given in Fig.10.
2. At start-up of the oscillator.

AC CHARACTERISTICS

V_{DD} = 3.3 V; V_{SS} = 0 V; T_{amb} = 25 °C; f_{osc} = 48 MHz; f_s = 44.1 kHz; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Driver characteristics D+ and D– (full-speed mode)						
t_r	rise time	C_L = 50 pF	4	–	20	ns
t_f	fall time	C_L = 50 pF	4	–	20	ns
$t_{rf(m)}$	matching rise/fall time (t_r/t_f)		90	–	110	%
V_{cr}	output signal crossover voltage		1.3	–	2.0	V
$R_{(o)driver}$	driver output resistance	steady-state drive	28	–	43	Ω
Data source timings D+ and D– (full-speed mode)						
$f_{i(sample)}$	audio sample input frequency		5	–	55	kHz
$f_{fs(D)}$	full-speed data rate		11.97	12.00	12.03	Mbits/s
t_{fr}	frame interval		0.9995	1.0000	1.0005	ms
$t_{J1(dif)}$	source differential jitter to next transition		–3.5	0.0	+3.5	ns
$t_{J2(dif)}$	source differential jitter for paired transitions		–4.0	0.0	+4.0	ns
$t_{W(EOP)}$	source End Of Packet (EOP) width		160	–	175	ns
$t_{EOP(dif)}$	differential to EOP transition skew		–2.0	–	+5.0	ns
t_{JR1}	receiver data jitter tolerance to next transition		–18.5	0.0	+18.5	ns
t_{JR2}	receiver data jitter tolerance for paired transitions		–9.0	0.0	+9.0	ns
t_{EOPR1}	EOP width at receiver must reject as EOP		40	–	–	ns
t_{EOPR2}	EOP width at receiver must accept as EOP		82	–	–	ns
Serial input/output data timing; see Fig.7						
$f_{clk(sys)}$	system clock frequency		–	12	–	MHz
$f_{i(WS)}$	word select input frequency		5	–	55	kHz
t_r	rise time		–	–	20	ns
t_f	fall time		–	–	20	ns
$t_{BCK(H)}$	bit clock HIGH time		55	–	–	ns
$t_{BCK(L)}$	bit clock LOW time		55	–	–	ns
$t_{s;DAT}$	data set-up time		10	–	–	ns
$t_{h;DAT}$	data hold time		20	–	–	ns
$t_{s;WS}$	word select set-up time		20	–	–	ns
$t_{h;WS}$	word select hold time		10	–	–	ns

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
SDA and SCL lines (standard I^2C-bus); see Fig.5						
f_{SCL}	SCL clock frequency		0	–	100	kHz
t_{BUF}	bus free time between a STOP and START condition		4.7	–	–	µs
$t_{HD;STA}$	hold time (repeated) START condition		4.0	–	–	µs
t_{LOW}	SCL LOW time		4.7	–	–	µs
t_{HIGH}	SCL HIGH time		4.0	–	–	µs
$t_{SU;STA}$	set-up time for a repeated START condition		4.7	–	–	µs
$t_{SU;STO}$	set-up time for a STOP condition		4.0	–	–	µs
$t_{HD;DAT}$	data hold time		5.0	–	0.9	µs
$t_{SU;DAT}$	data set-up time		250	–	–	ns
t_r	rise time of both SDA and SCL signals		–	–	1000	ns
t_f	fall time of both SDA and SCL signals		–	–	300	ns
$C_{L(bus)}$	load capacitance for each bus line		–	–	400	pF
Oscillator; note 1						
f_{osc}	oscillator frequency		–	48	–	MHz
δ	duty factor		–	50	–	%
g_m	transconductance		13.5	23.0	30.5	mS
R_o	output resistance		450	700	1450	Ω
$C_{i(XTAL1)}$	parasitic input capacitance at XTAL1		10	11	12	pF
$C_{i(XTAL2)}$	parasitic input capacitance at XTAL2		4.5	5.0	5.5	pF
I_{start}	start current		4.3	8.8	15.0	mA
Power-on reset						
$t_{su(POR)}$	power-on reset set-up time	notes 2 and 3	$5C_{ref}$	–	–	ms
Filter Stream DAC (FSDAC)						
RES	resolution		16	–	–	bits
$V_{o(FS)(rms)}$	full-scale output voltage (RMS value)	V_{DD} = 3.3 V	–	0.66	–	V
SVRR	supply voltage ripple rejection of V_{DDA} and V_{DDO}	f_{ripple} = 1 kHz; $V_{ripple(p-p)}$ = 0.1 V	–	60	–	dB
$\lvert\Delta V_o\rvert$	channel unbalance	maximum volume	–	0.03	–	dB
α_{ct}	crosstalk between channels	R_L = 5 kΩ	–	95	–	dB

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
(THD + N)/S	total harmonic distortion-plus-noise to signal ratio	f_s = 44.1 kHz; R_L = 5 kΩ				
		at input signal of 1 kHz (0 dB)	–	–90[4]	–80	dB
			–	0.0032	0.01	%
		at input signal of 1 kHz (–60 dB)	–	–30[4]	–20	dB
			–	3.2	10	%
S/N_{bz}	signal-to-noise ratio at bipolar zero	A-weighted at code 0000H	90	95	–	dBA

Notes

1. A 3rd overtone crystal of 48 MHz must be used in combination with a filter connected to the oscillator output (XTAL2), (L = 1.5 µH ±10%; C = 10 nF ±10%). The series resistance of the crystal must be below 60 Ω. C_{xtal1} = 4.7 pF ±10%; C_{xtal2} = 12 pF ±10%).
2. Strongly depends on the external decoupling capacitor connected to V_{ref}.
3. Use for calculation of the power-on reset set-up time the C_{ref} value in µF.
4. The audio information from the USB interface is fed directly to the ADAC.

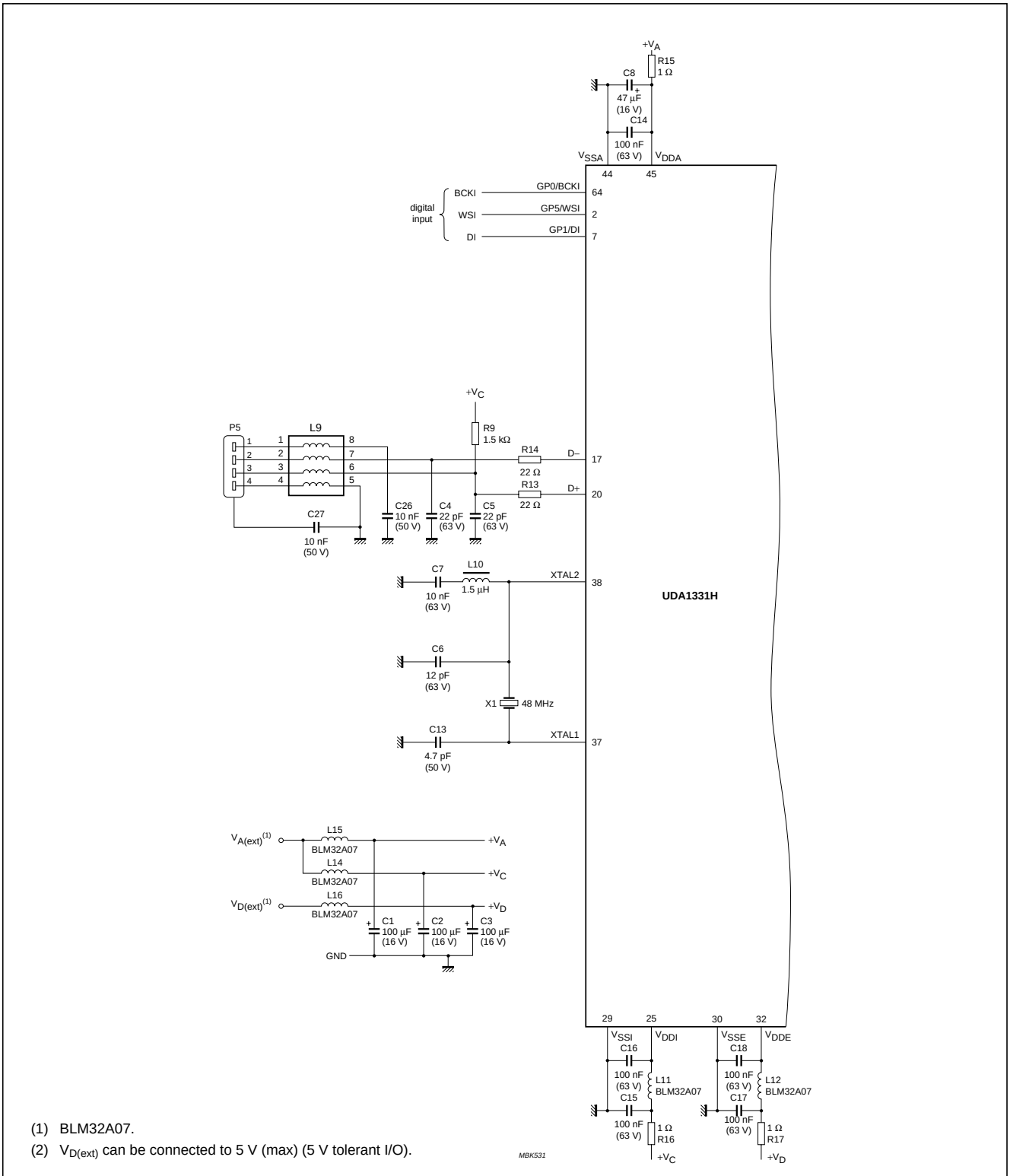
APPLICATION INFORMATION

The UDA1331H can only be used in combination with an external (E)PROM. This (E)PROM can be connected to the port pins (P0 and P2) of the UDA1331H and must contain the firmware for the microcontroller. The UDA1331H will be delivered with standard USB compliant firmware.

The I^2C-bus EEPROM is optional and can be used to configure client specific configurations and descriptors.

More information about the firmware, descriptors and configurations can be obtained from several application notes.

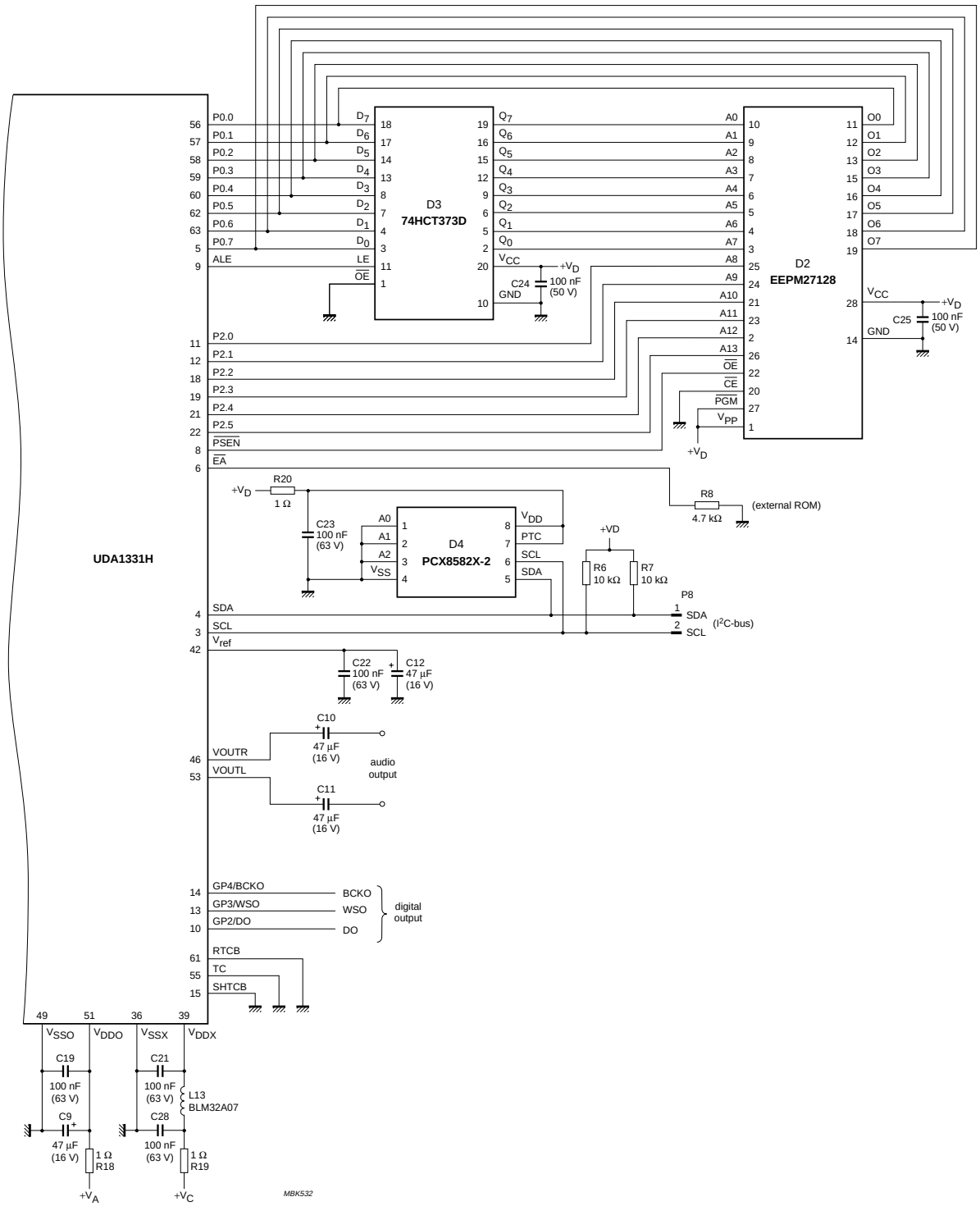
APPLICATION DIAGRAM



(1) BLM32A07.

(2) $V_{D(ext)}$ can be connected to 5 V (max) (5 V tolerant I/O).

Fig.9 Application diagram (continued in Fig.10).

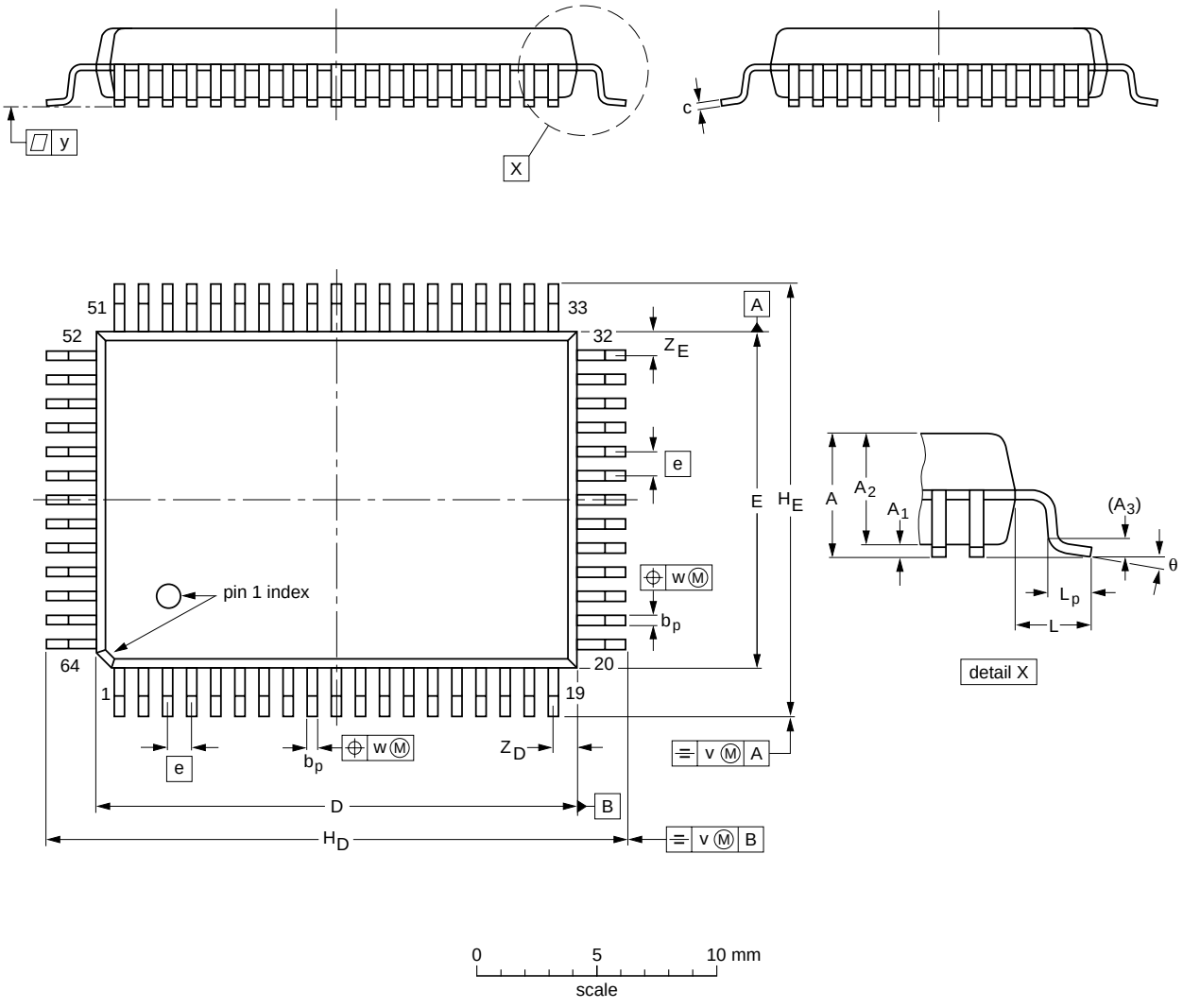


(1) BLM32A07.

Fig.10 Application diagram (continued from Fig.9).

PACKAGE OUTLINE

QFP64: plastic quad flat package; 64 leads (lead length 1.95 mm); body 14 x 20 x 2.8 mm **SOT319-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	3.20	0.25 0.05	2.90 2.65	0.25	0.50 0.35	0.25 0.14	20.1 19.9	14.1 13.9	1	24.2 23.6	18.2 17.6	1.95	1.0 0.6	0.2	0.2	0.1	1.2 0.8	1.2 0.8	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT319-2						~~95-02-04~~ 97-08-01

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all QFP packages.

The choice of heating method may be influenced by larger plastic QFP packages (44 leads, or more). If infrared or vapour phase heating is used and the large packages are not absolutely dry (less than 0.1% moisture content by weight), vaporization of the small amount of moisture in them can cause cracking of the plastic body. For more information, refer to the Drypack chapter in our *"Quality Reference Handbook"* (order code 9397 750 00192).

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several methods exist for reflowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 50 and 300 seconds depending on heating method. Typical reflow peak temperatures range from 215 to 250 °C.

Wave soldering

Wave soldering is **not** recommended for QFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

CAUTION
Wave soldering is NOT applicable for all QFP packages with a pitch (e) equal or less than 0.5 mm.

If wave soldering cannot be avoided, for QFP packages with a pitch (e) larger than 0.5 mm, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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